

Powerboard Plans and Challenges

US Strip Meeting - May 11th 2016

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- **30 PBs in total** for the US, 10 at LBNL, 20 at Liverpool; Modification can be done at either location
- Current TM PB do not allow to program the FEAST output voltage → Could use **digital potentiometer**
- No suitable I-wire digital pot available → Use **I-wire to I2C** translator
- Will need more real estate → Design PCB which fits into the HVmux space → **Who?** Ashley tentatively said he could do it.
- This board would also allow to host an ADC to measure temperature of the FEAST
- But: **need to power the additional board**, current will be low, but dropping from 10V will still dissipate some heat, is that OK?
- Other ideas or wishes?

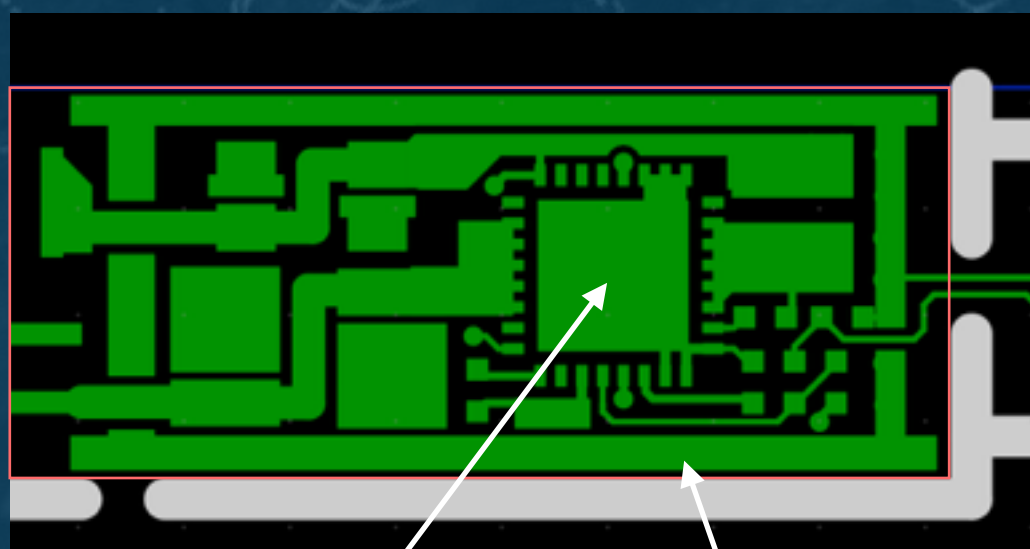
- Ashley expressed the wish to have a **PBv1 retro fitted with an AMAC**
- Use HVmux real estate to deploy carrier PCB for AMAC
- AMAC powered by its **own LDO**
- Replace **I-wire functionality with AMAC**, will need flywires to control AMAC with I2C, this is not intended for stave usage
- Checking design if more functionality of the AMAC can be used (e.g. measure current or voltage)
- Main purpose of this test: **check if HV current measuring scheme adds noise to the module!**
- Personal note: this PCB would basically do what we want to do with PBv2, could only focus on PBv2 and skip this. Opinions?

UpFEAST Size:

- UpFeast die is **larger** than current FEAST and will require a bigger package
- This might be challenging as there is very **little space left**
- Actually wanted more space to make shield soldering easier
- Using **bare die does not seem to be an option**, as they only get tested once they packaged

Shield box mounting:

- Shield nearly as wide as PB
- Not a lot of **space left for soldering**
- Fully enclosed shield important, see AUW talk
- Need to keep this in mind for production, suggestion: laser welding, would also get rid of copper coating (solely for soldering)
- Generally would **like flatter design**



9 mm



Feast

Shield Pad

TID bump:

- Long story short: the **digital current** of all GF130nm chips will increase by factor 2.5 (as of latest measurements)
- This factor will **affect only 2% of the detector lifetime** (up to ~5MRad)
- Detector (probably) needs to be biased to surpass bump (makes pre-irrad not unrealistic)
- Two options:
 - **Over-design** system to accommodate for current scaling factor
 - **Mitigate** current or scale factor

Over-designing:

- **Feast can be designed for higher current** (also higher efficiency at higher current)
- But in designing for higher current we will increase the mass, as all components and traces have to be adapted (higher current → more copper)
- **Dual-Feast does not seem realistic** due to space concerns (or can we expand in 3D ?)
- Keep thermal characteristics in mind, can we cope with them?

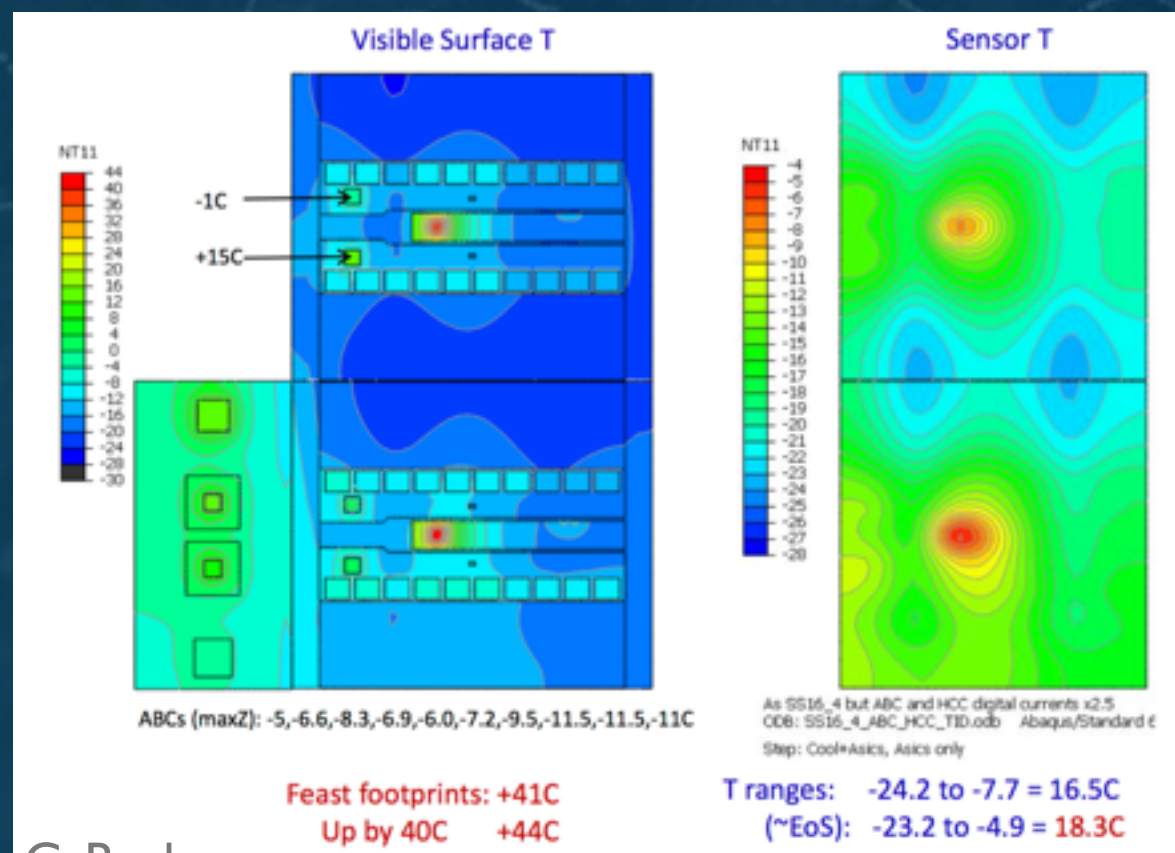
Mitigating the bump:

- 1 of 2 TSMC 130nm foundries has shown not to have the TID bump feature (to be validated by end of this month)
- Can we **migrate the HCC* into TSMC 130nm**? Digital only should be relatively “easy”? Would result in 1A less!
- **ABC* migration unrealistic** due to analog design?
- Can we **decrease the digital current in other ways**? Reduce supply voltage? Clock gating? Only need this for 2% of the time!

Short Strip Module (estimates)				
	Nominal		x2.5	
	Digital	Analog	Digital	Analog
2 x HCC*	660mA	0mA	1650mA	0mA
20 x ABC*	700mA	1100mA	1750mA	1100mA
Total	2460mA		4500mA	

Thermal Issues:

- Current thermal simulations show huge **temp. gradients of up to 20°C** under FEAST and HCC
- To be checked if this is Ok for the sensor
- Can we **improve this with a different PB design?**
 - Move Feast seems impractical due to clearance
 - Different board material? BeO?
 - BeO heat spreader under PB?



Switching Noise:

- Need more studies of PBs on modules
- Important feedback for design
- **How will the LDOs inside the Feast behave?** Do we have space for enough filtering
- How does the **EMR behave under high currents and/or after irradiation**
- How do different assembly procedures perform in respect to EMR?

Integration:

- Do we need to **control glue height?**
- If yes we need to glue PB to the module with similar techniques as hybrids
- Tooling will depend on PB shape

Reliability:

- Reliability testing needs lots of time
- **Only conclusive with final design** and chips
- Will need to wait for most issues to be solved
- Prototype stress testing is good, but final assembly process is what might affect reliability most

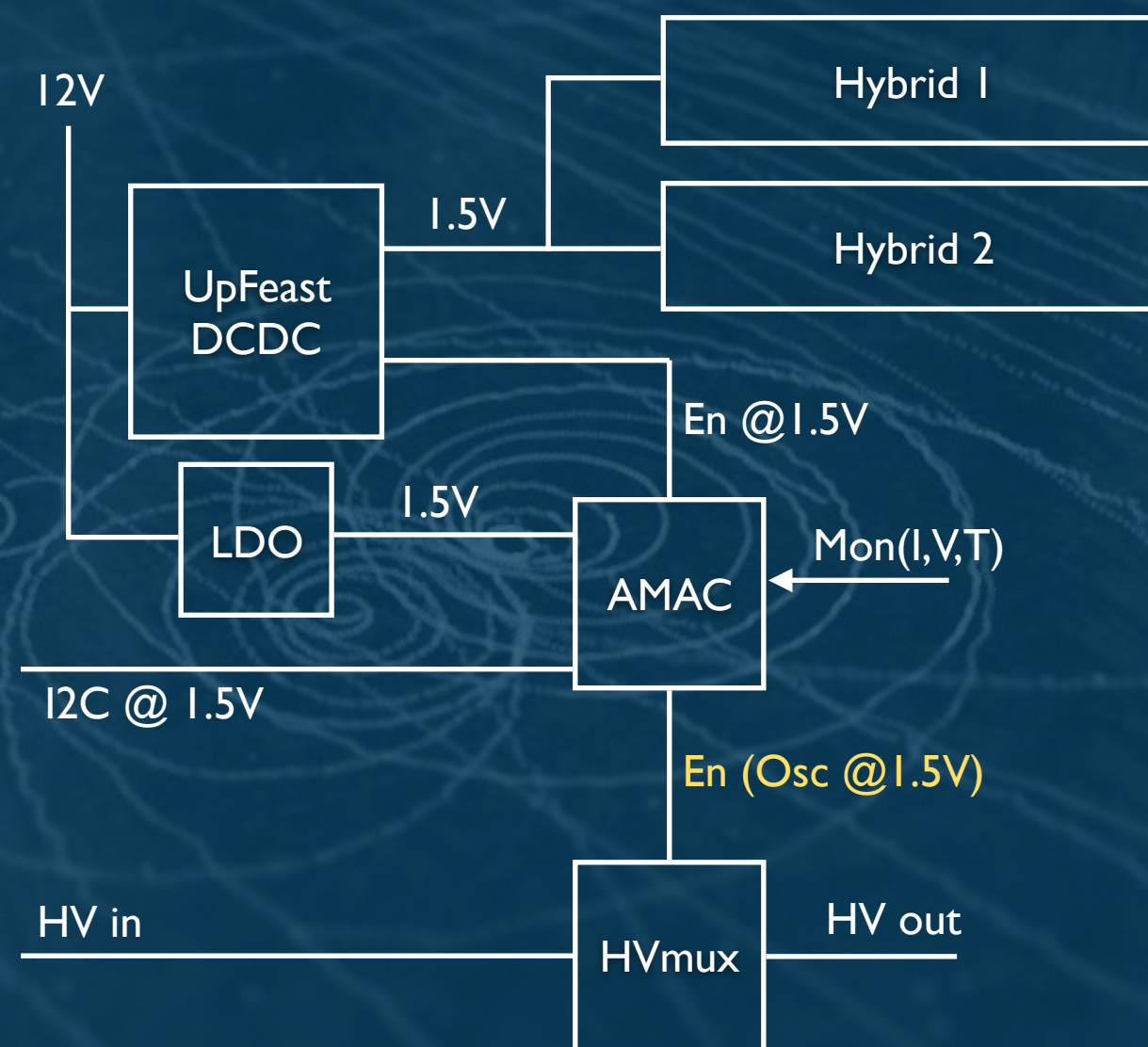
G. Beck

Specs:

- UpFeast (if possible, when will it be available?) 1.5V output
- Same DCDC circuit
- **AMAC with its own LDO** (1.5V) and monitoring fully hooked up (How to access interrupts?)
- HVmux circuit on board
- HV connection scheme still open
- Is a **second LDO for different IO voltage needed?**
- Would like perform stress testing on final PCB material

Panelisation:

- Would like to have a **wirebond-less** way of having test connections on each PB
- Could route **traces through perforation**, but this would leave an **open trace on the side after cutting**, probably not good close to the sensor
- Use **bed-of-nail type** connection?
- Starting communication with vendor



- Currently preparing for AMAC testing which will tie in with producing PBv2 (or retro-fitting PBv1)
- **Total of ~40 AMACs will be available**, Penn & LBNL need around 10 for prototype testing and irradiation
- Would like to equip a half/full PBv2 panel (~15 boards) for testing of production chain and panelisation → These PBs will become available at some point, but I will use them initially for testing (and possibly stress testing)
- Hoping to **have stuffed PBv2 available by September**, is that early enough? (First prototypes hopefully around August)
- **Setup and exercise production chain** till end of 2016
- Do we want to test something on this board?